Design and implementation of Gigabit 0.25μm CMOS Transimpedance amplifier(TIA) for Optical Receiver Application

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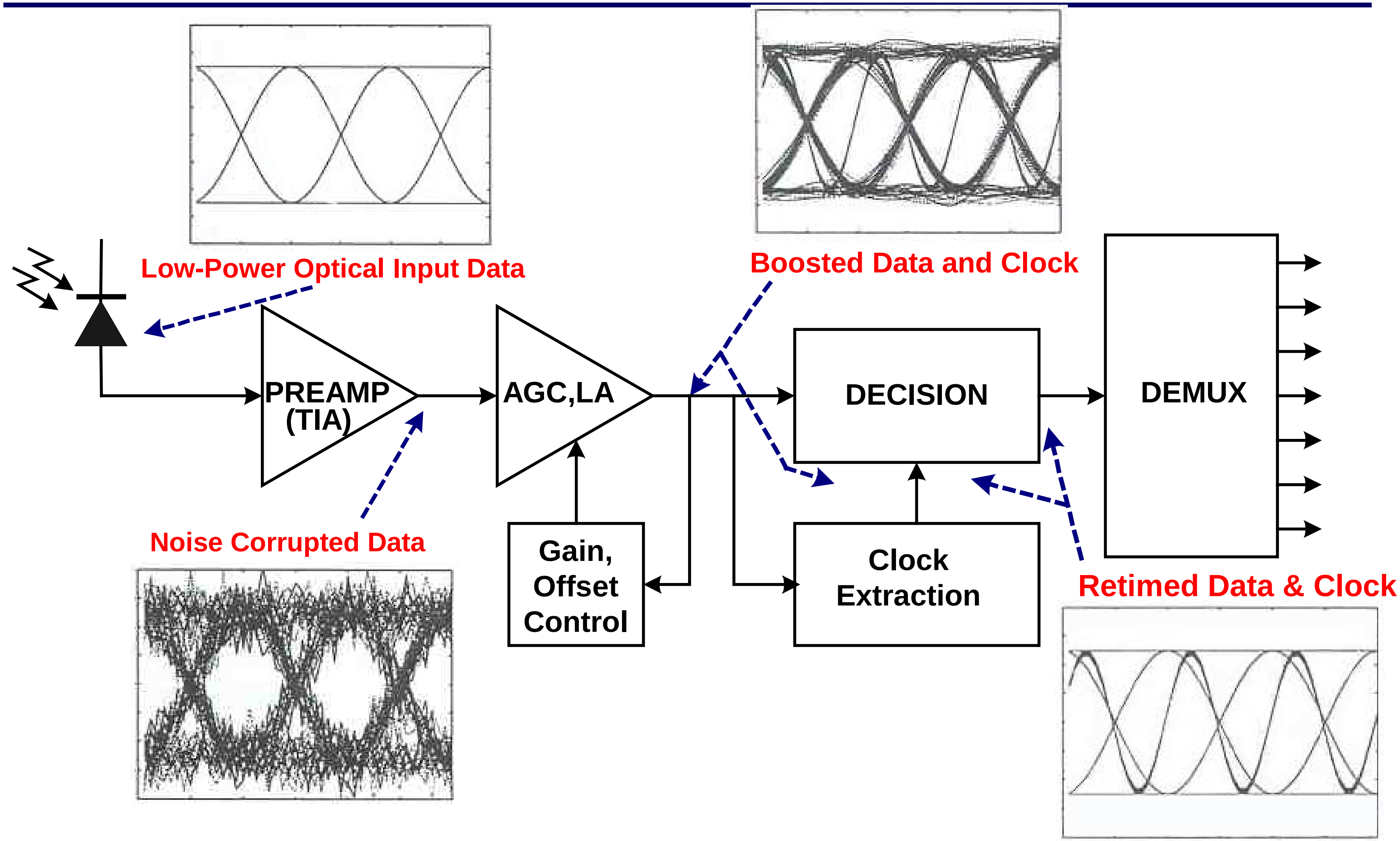
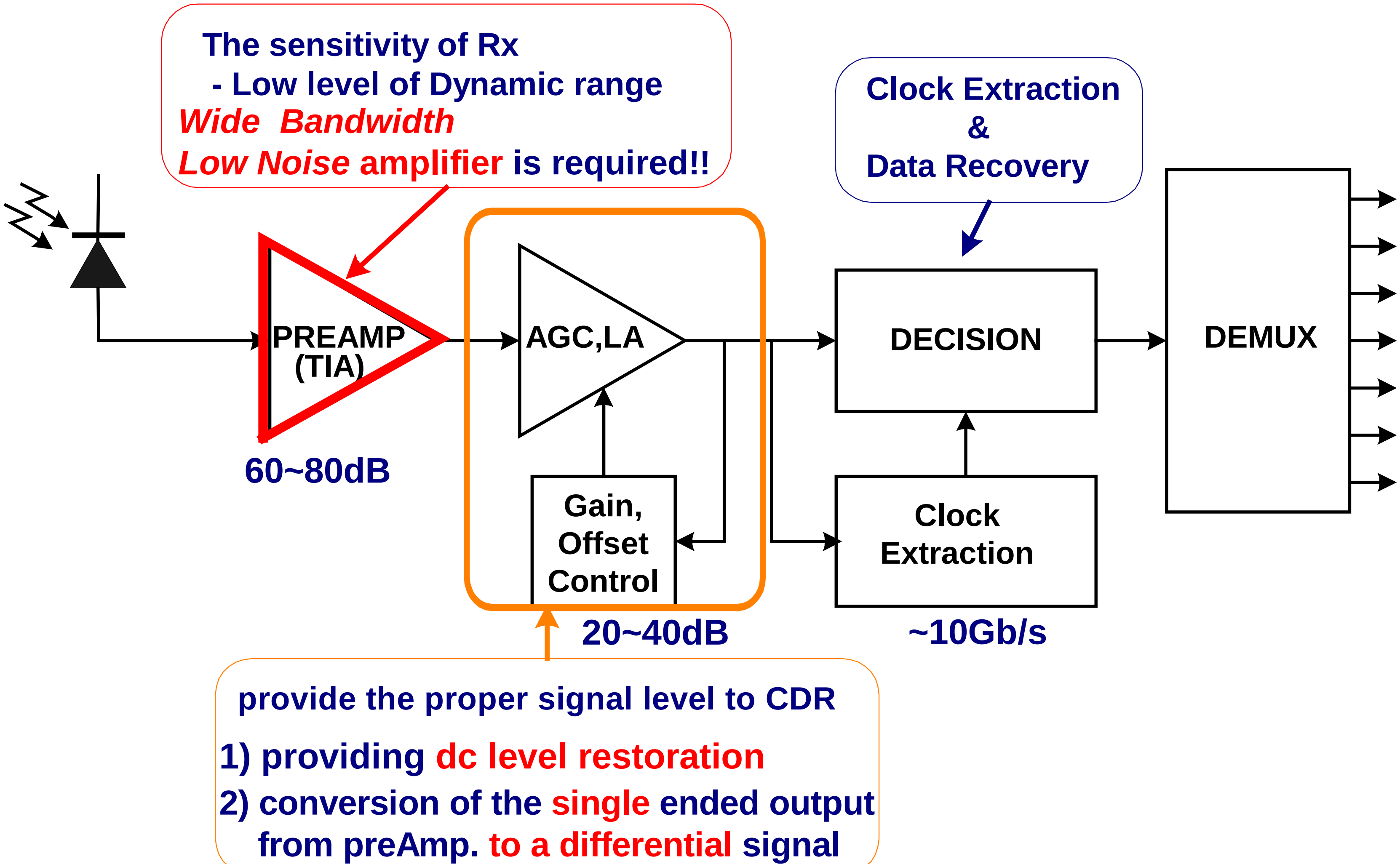
Outline

- Motivation
  - Overview of optical receiver
  - Design goal
- Transimpedance Amplifier (TIA)
- Conventional Approaches
- Proposed Approaches
- Measurement results
- Conclusions

What is Optical Receiver?



Overview of Optical Rx Design



Design Goal

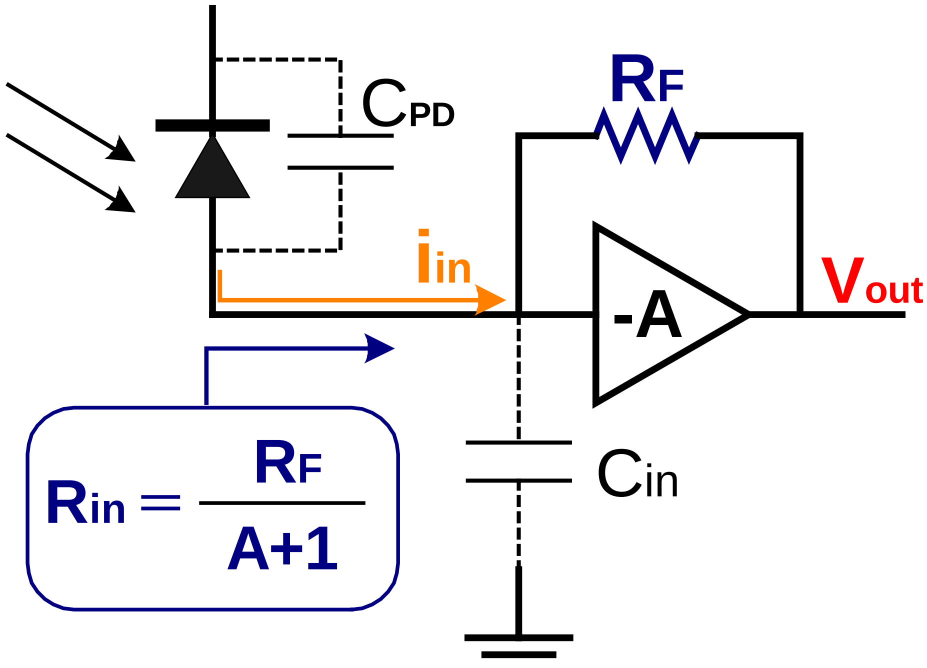
- Gain range : 60~80dB (1kΩ ~ 10kΩ)
- Wide bandwidth
- Low Noise
- Fully Differential Preamplifier
- CMOS implementation

Outline

- Motivation
- **Transimpedance Amplifier (TIA)**
  - **Why TIA?**
  - **Noise Source**
  - **TIA Noise & Design Solution**
- Conventional Approaches
- Proposed Approaches
- Measurement results
- Conclusions

Why Transimpedance amp.?

- Transimpedance front-end



$$R_{in} = \frac{R_F}{A+1}$$

$$Z_T(s) = R_T \frac{1}{1+sT}$$

$$R_T = \frac{A}{A+1} R_F$$

$$BW = \frac{1}{2\pi} \frac{A+1}{R_F C_T}$$

$$C_T = C_{PD} + C_{in}$$

Noise Source (1/5)

- **Shot Noise**
- **Thermal Noise**
- **Frequency Dependent Noise**
- **Digital noise through same substrate**

Noise Source (2/5)

- **Shot noise**
  - Due to the random variations
  - The ultimate limiting factor
  - Power spectral density :

$$S_{shot}(f) = 2qI \quad [A^2/Hz]$$

  - Rms noise current :

$$i_{rms} = \sqrt{2qI \cdot BW} = \sqrt{2qI/\tau_{BW}}$$

Noise Source (3/5)

- **Thermal Noise**
  - Due to the kinetic energy of charged particles
  - Power spectral density :

$$S_{thermal}(f) = \frac{4kT}{R} \quad [A^2 / Hz]$$

  - noise current :

$$i_n^2 = \frac{4kT}{R}$$

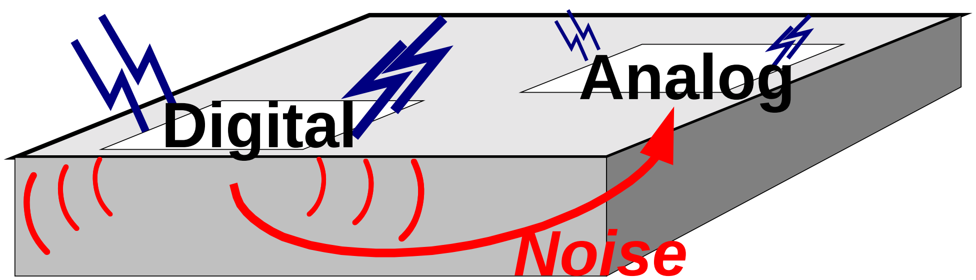
Noise Source (4/5)

- **Frequency Dependent Noise**
  - **Flicker noise (1/f noise)**
  - dependent upon the choice of materials, the processing purity
  - @ f=fcorner :

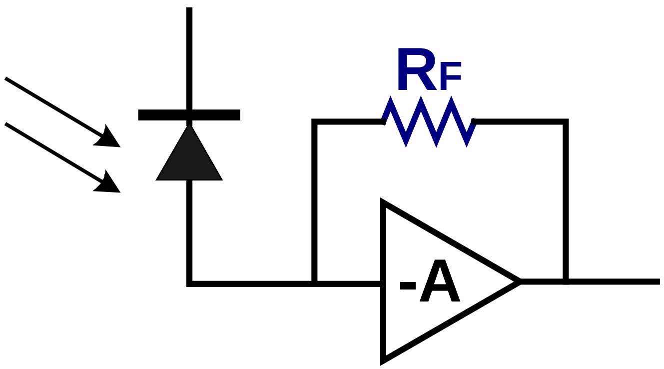
    Flicker noise = White noise in the device
  - Negligible with the broadband receivers.

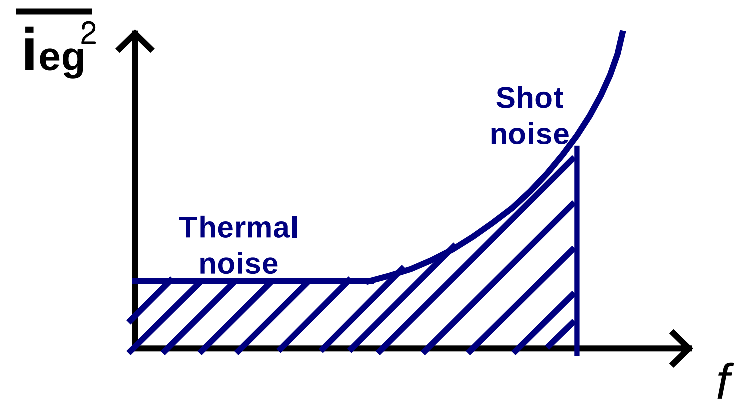
Noise Source (4/5)

- **Digital noise**
  - **Through same substrate of System On Chip**
  - **Switching noise**
  - **Signal induced noise**



TIA Noise & Design Solution





$$S_{nf}(f) = \frac{4kT}{R_F} + \left[2qI + \frac{4kT}{R_{in}}\right]\left(\frac{2\pi f C_T}{g_m}\right)^2$$

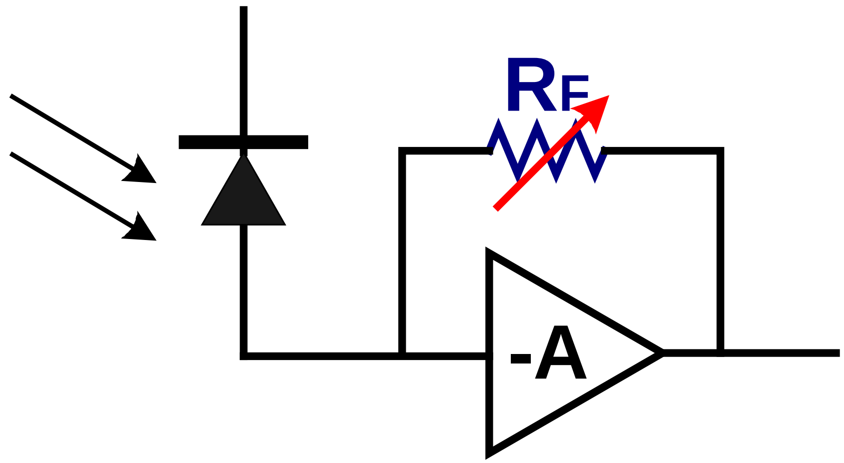
$$= \frac{4kT}{R_F} + \frac{w^2 C_T^{\ 2}}{g_m}\left[\frac{4kT}{R_{in}} + 2qI\right]$$

- ***Increase g_m, R_{in}, Decrease C_T !!***

Outline

- Motivation
- Transimpedance Amplifier (TIA)
- **Conventional Approaches**
  - **Wide dynamic techniques**
  - **Wide bandwidth techniques**
    - **Shunt peaking**
    - **Common gate input stage**
- Proposed Approaches
- Measurement results
- Conclusions

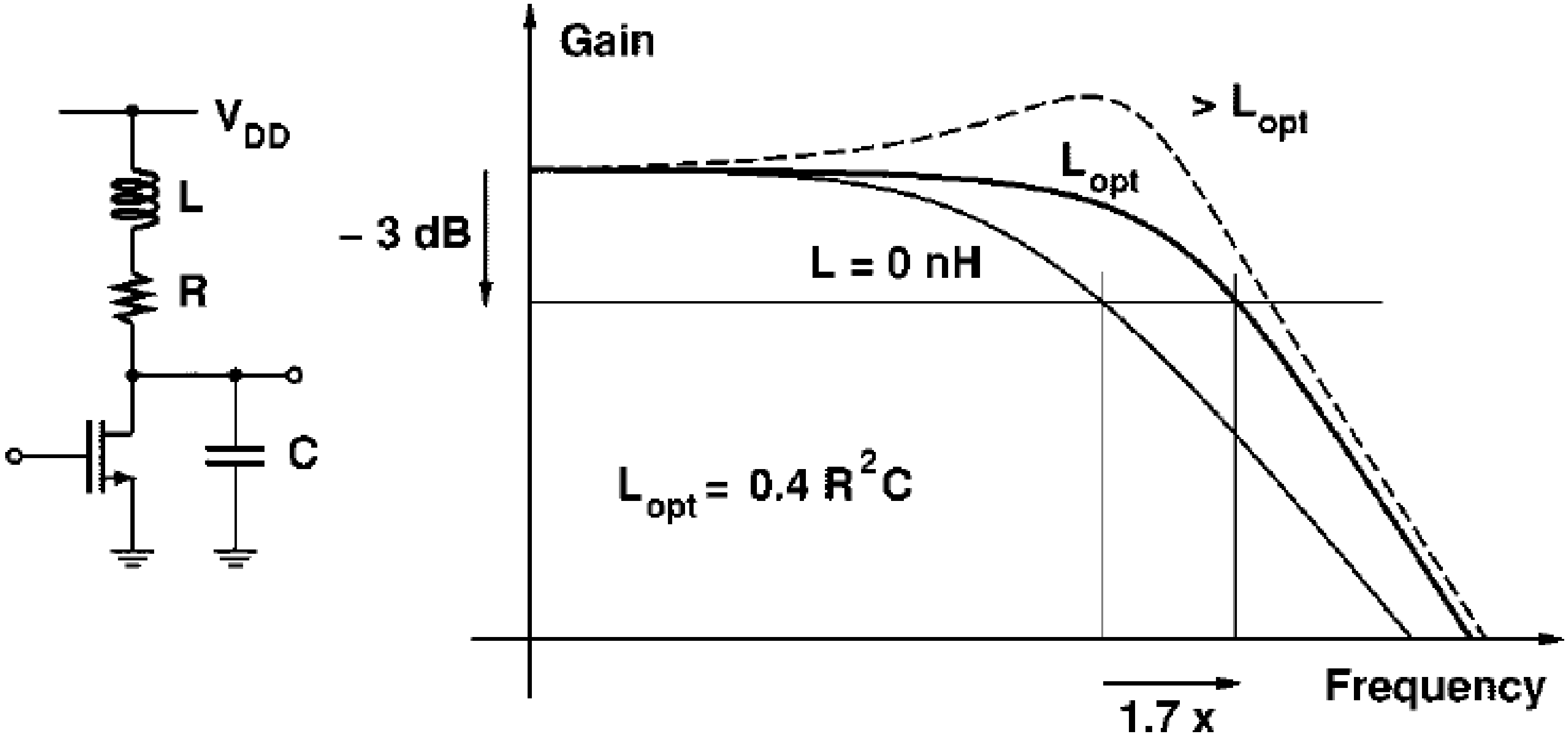
Wide dynamic range technique



- **Adaptive Transimpedance**
  - **Increased dynamic range**
  - **H. Khorramabadi ISSCC'95**
    - **A 1.06Gb/s, -31dBm to 0dBm BiCMOS optical preamplifier featuring adaptive transimpedance**
  - **K. Phang ISSCC'01**
    - **A 1V 1mW CMOS Front-End with On-Chip Dynamic Gate Biasing for a 75Mb/s Optical Receiver**

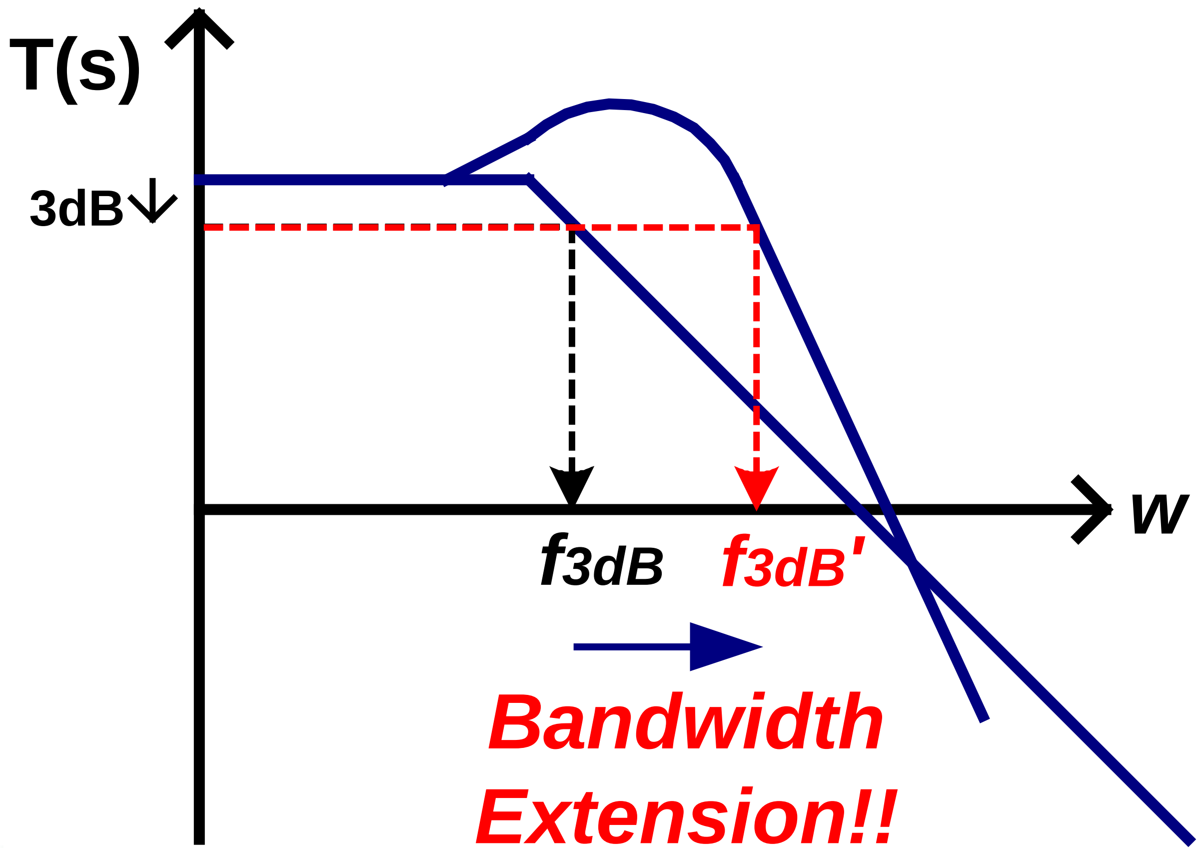
Wide bandwidth techniques(1/3)

- **Shunt peaking**

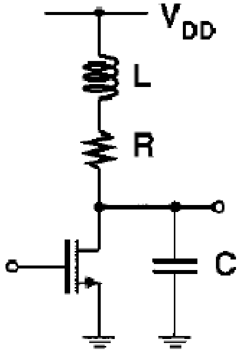


Wide bandwidth techniques(2/3)

- **Shunt peaking**
  - **Add zero**

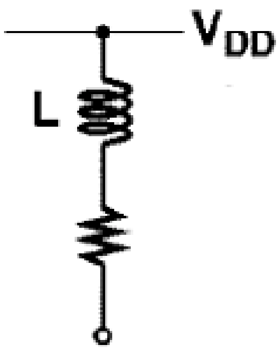


Wide bandwidth techniques(3/3)

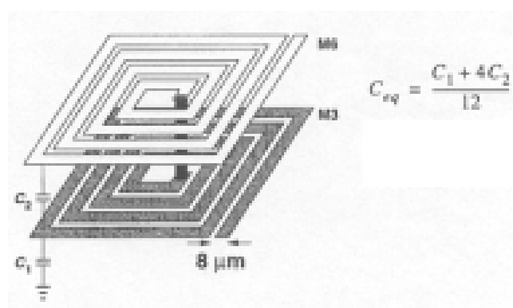


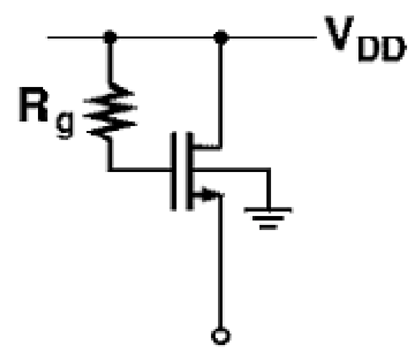
- **L-implementation :**
  - (a) Spiral inductors
  - (b) Active inductors

$$L = \frac{R_g}{\omega_T}$$



(a)



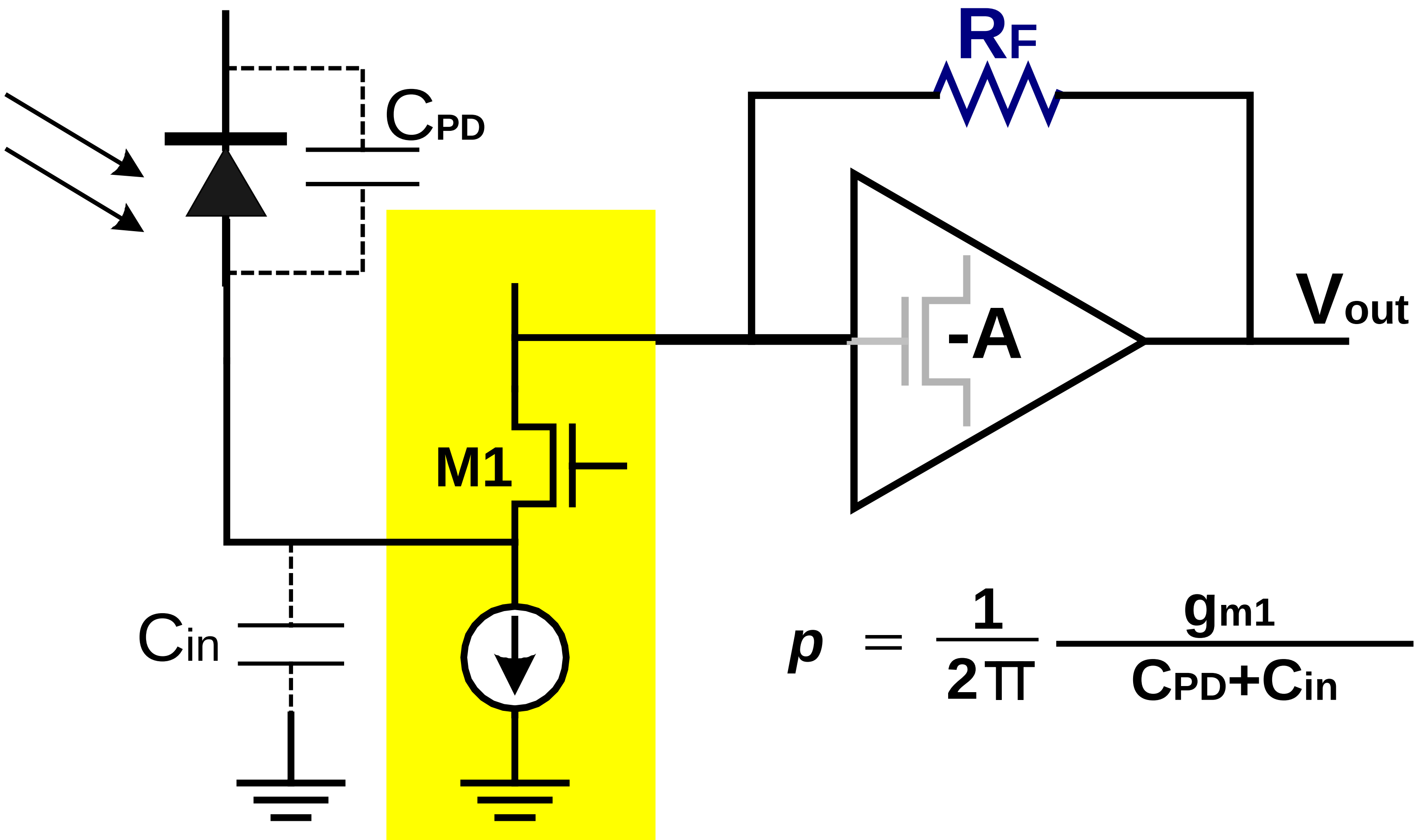


(b)

•(a) J. Savoj et al., "A 10Gb/s CMOS Clock and Data Recovery Circuit with Frequency Detection", ISSCC'01

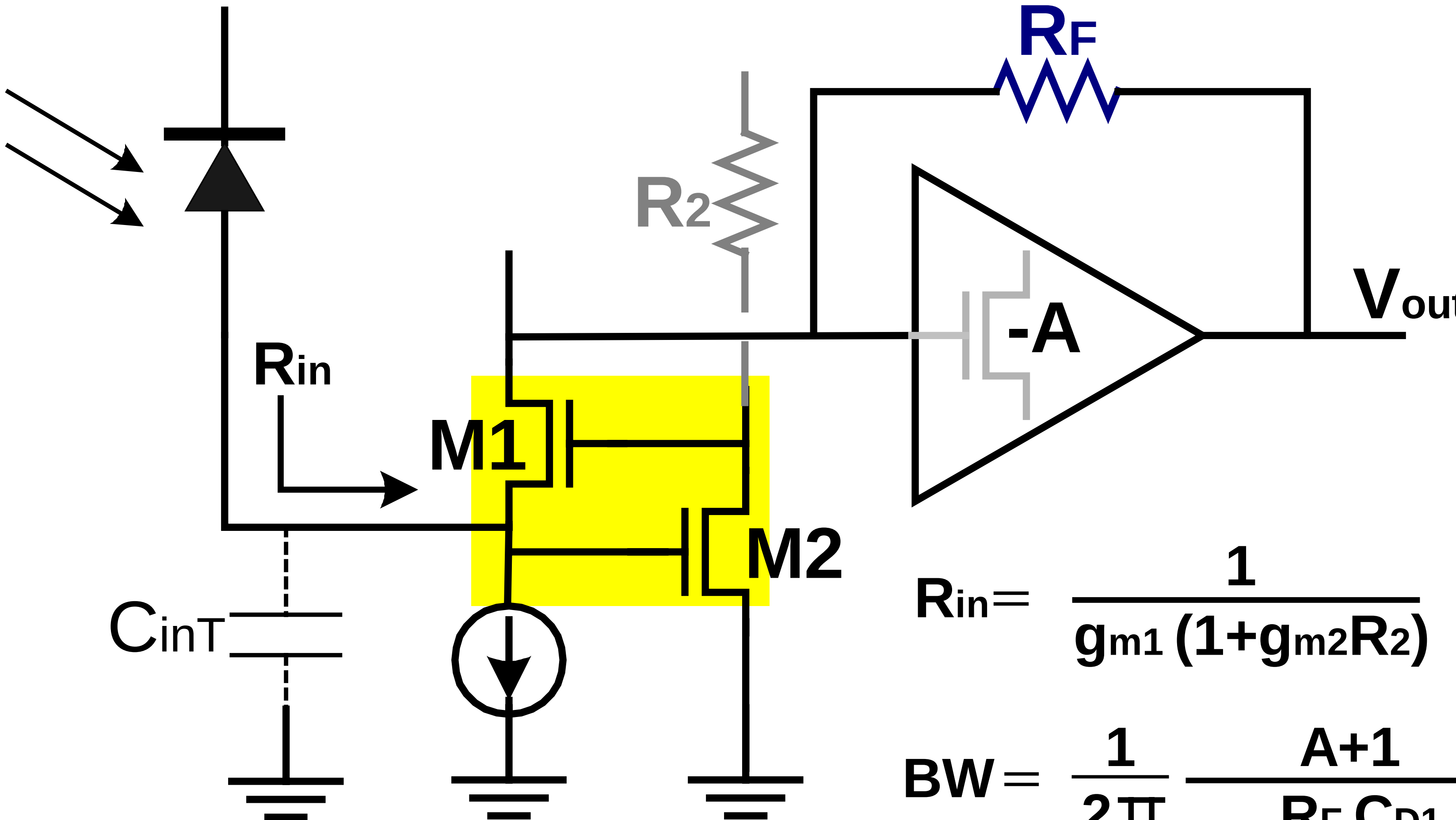
•(b) E. Säckinger et al., "A 3-GHz 32-dB CMOS Limiting Amplifier for SONET OC-Receivers" ISSCC'00

Common-Gate Input stage



$$p = \frac{1}{2\pi} \frac{g_{m1}}{C_{PD}+C_{in}}$$

Regulated-Cascode Input stage



$$R_{in} = \frac{1}{g_{m1}(1+g_{m2}R_2)}$$

$$BW = \frac{1}{2\pi}\frac{A+1}{R_F C_{D1}}$$

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- **Proposed Approaches**
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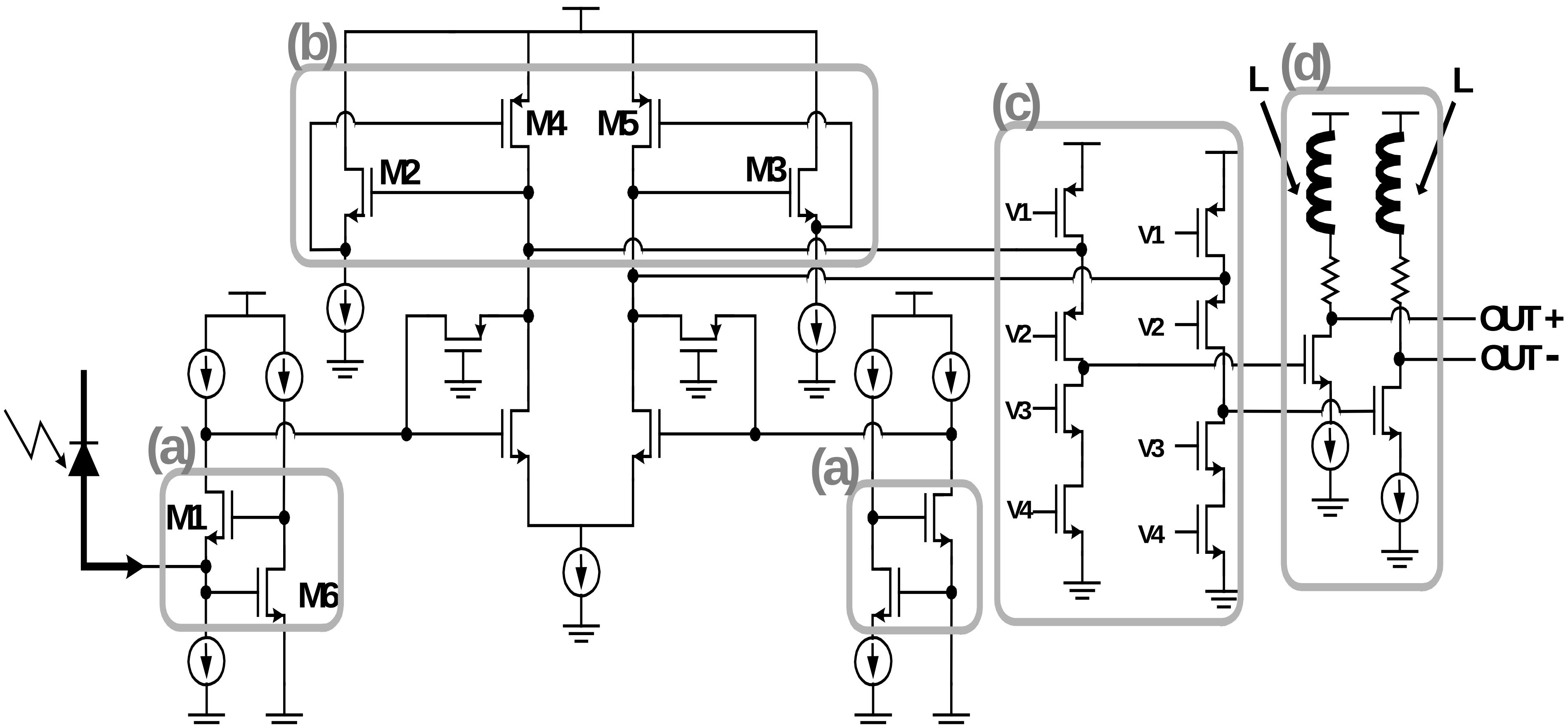
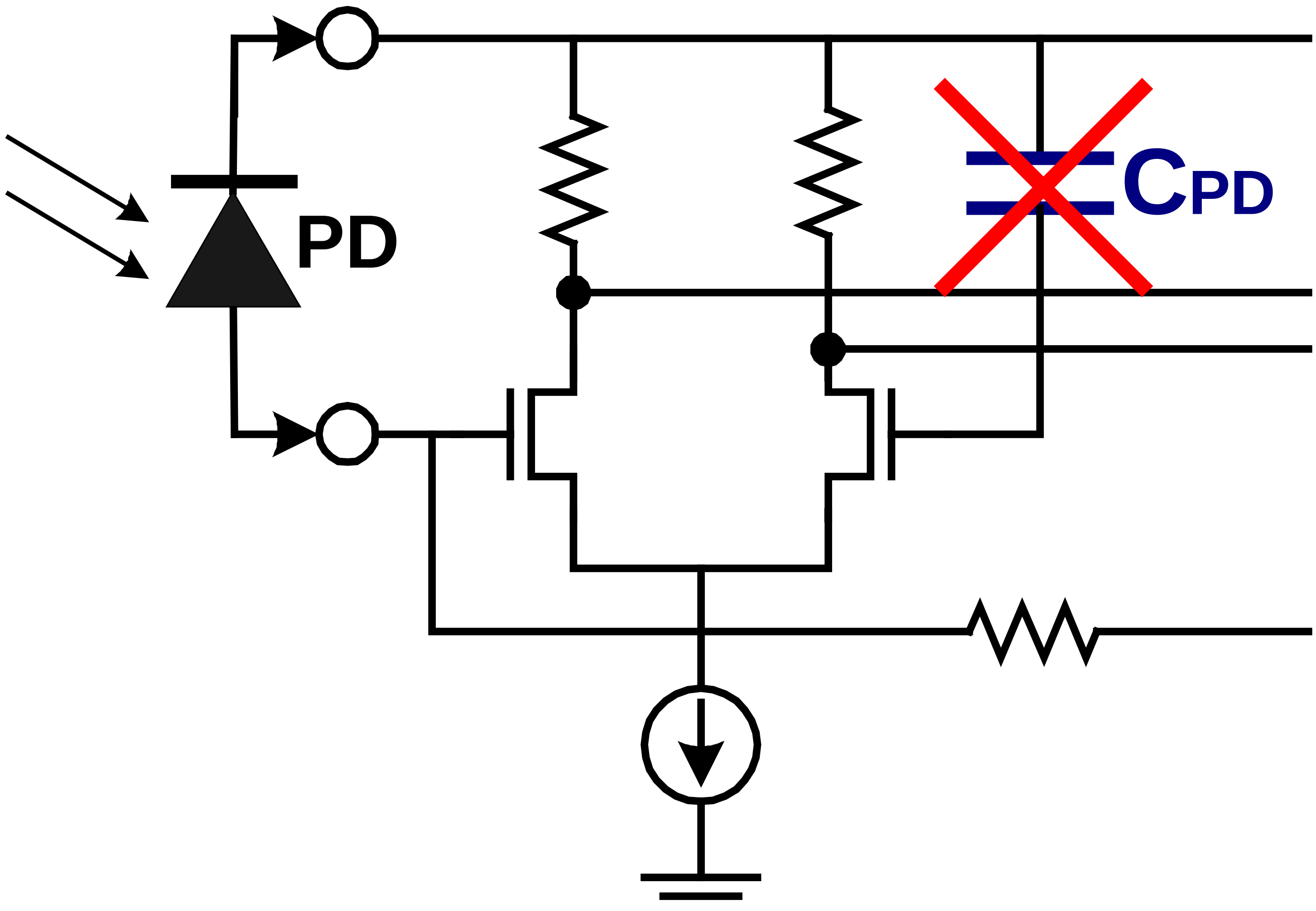
Proposed Structure(1/3)



Proposed Structure(2/3)

- Fully Differential configuration
- Regulated Cascode input stage
  - No need of the matching capacitor at the differential input stage due to PD
  - Bandwidth Enhancement Technique
- Wide swing technique
  - Conventional loads are replaced with Vth compensation loads.


PD
CPD

Proposed Structure(3/3)

- **Shunt peaking technique**
- **Low Noise technique**
  - **Regulated Cascode:**
    - **Increasing g_m which makes low noise characteristic**
  - **Substrate Bias Effects on the drain current**
- **Buffer replaced with cascoded stage**
  - **Amplifier ability (~20dBΩ differential) with DC level shifting**
  - **Low power consumption with high gain characteristic**

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- Motivation
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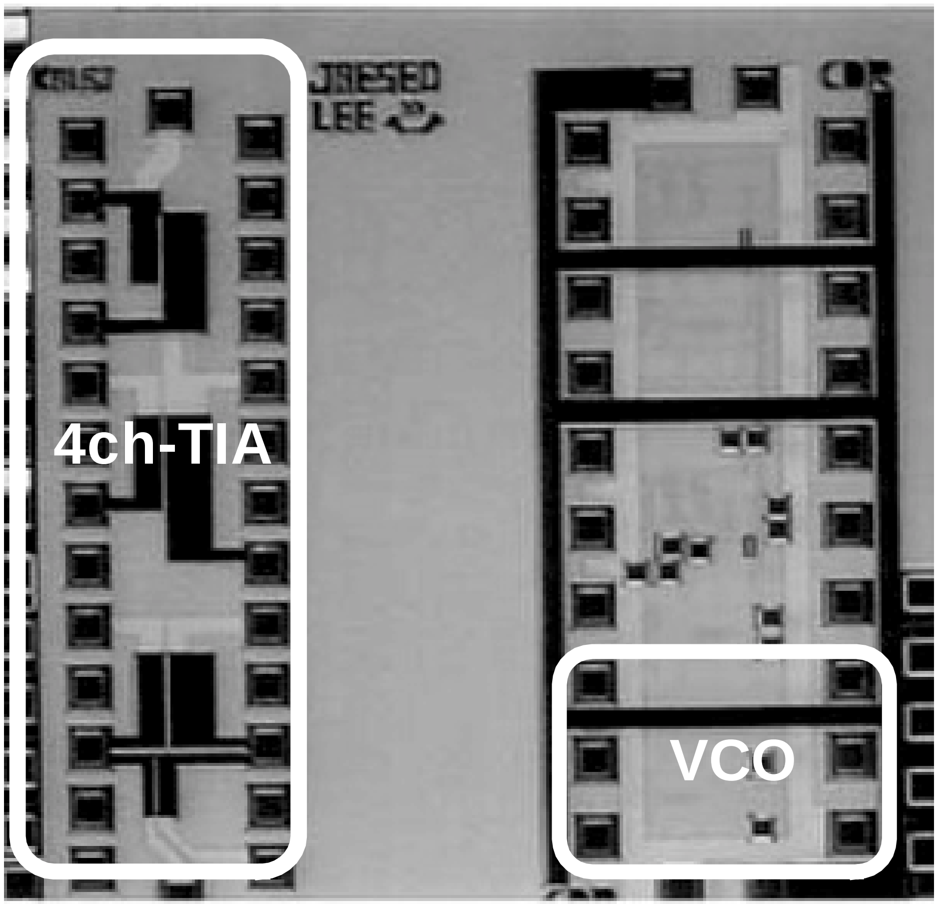
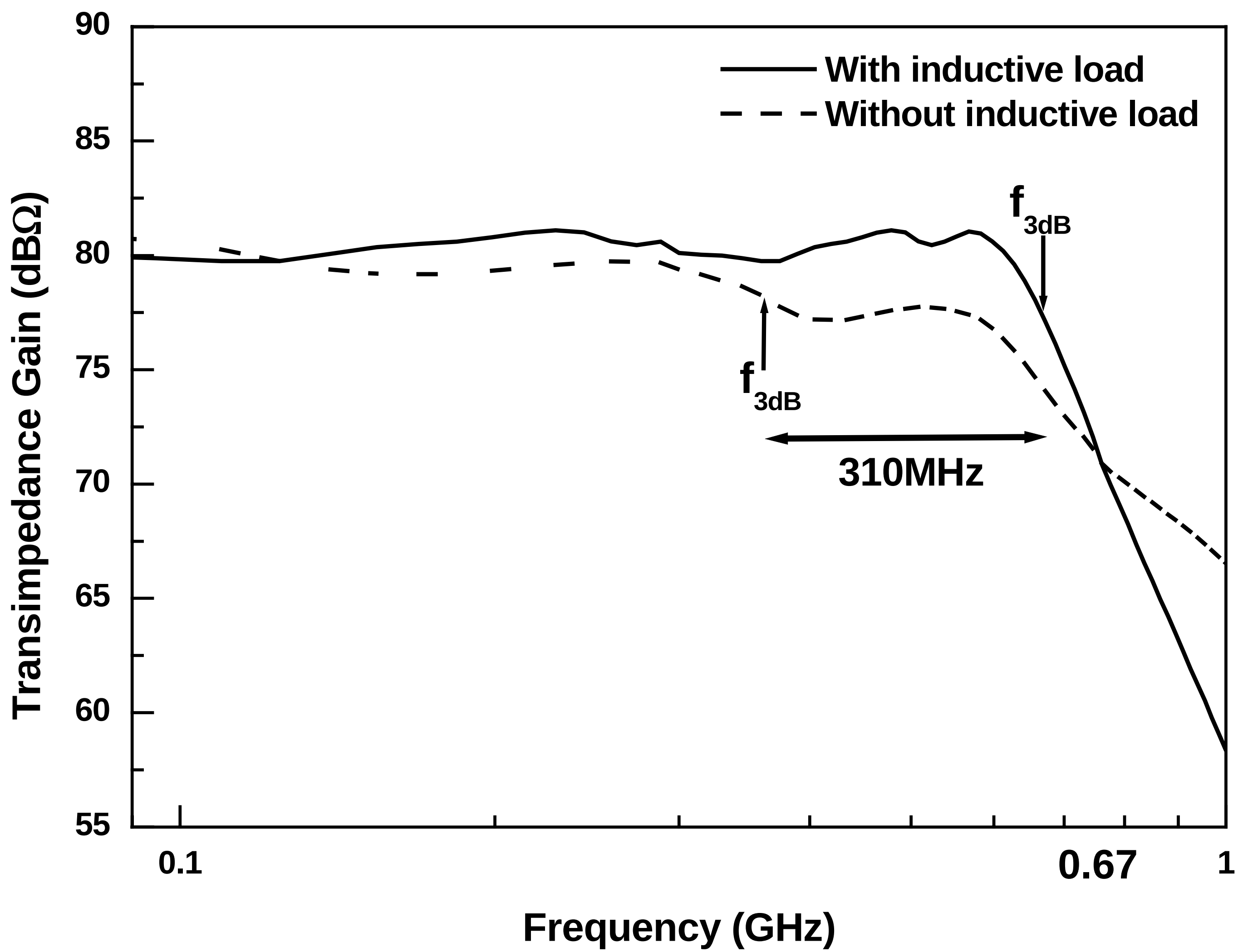
- Conventional Approaches
- Proposed Approaches
- **Measurement results**
  - Chip Microphotograph
  - Gain, Bandwidth, Crosstalk & Noise current
  - Digital Noise
  - Multichip Oxide Process Chip
  - Test boards
  - Eye diagrams
- Conclusions

Chip microphotograph

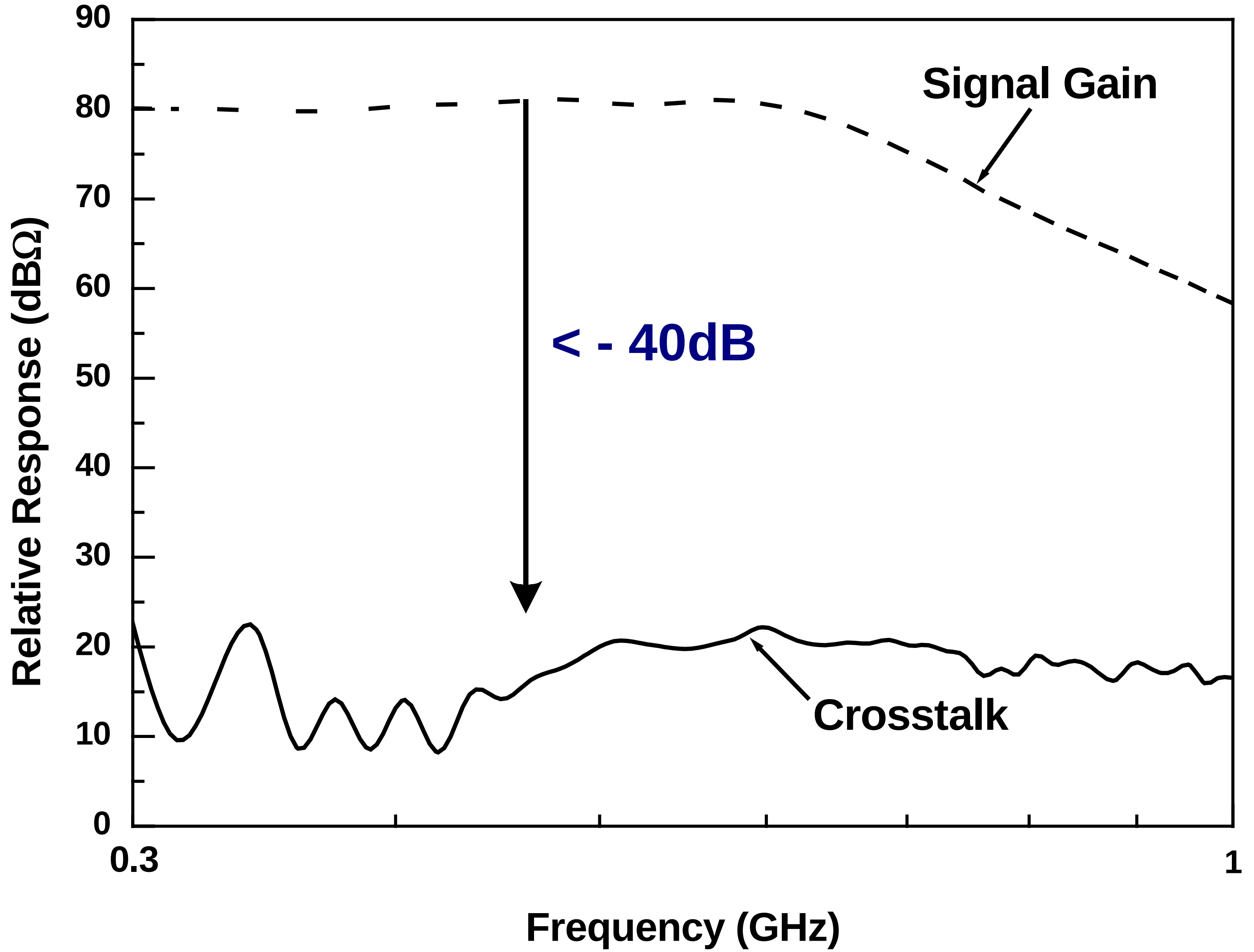


- 0.25μm Standard CMOS
- 1poly 5metal
- Retrograde twin well
- 2mm x 2mm

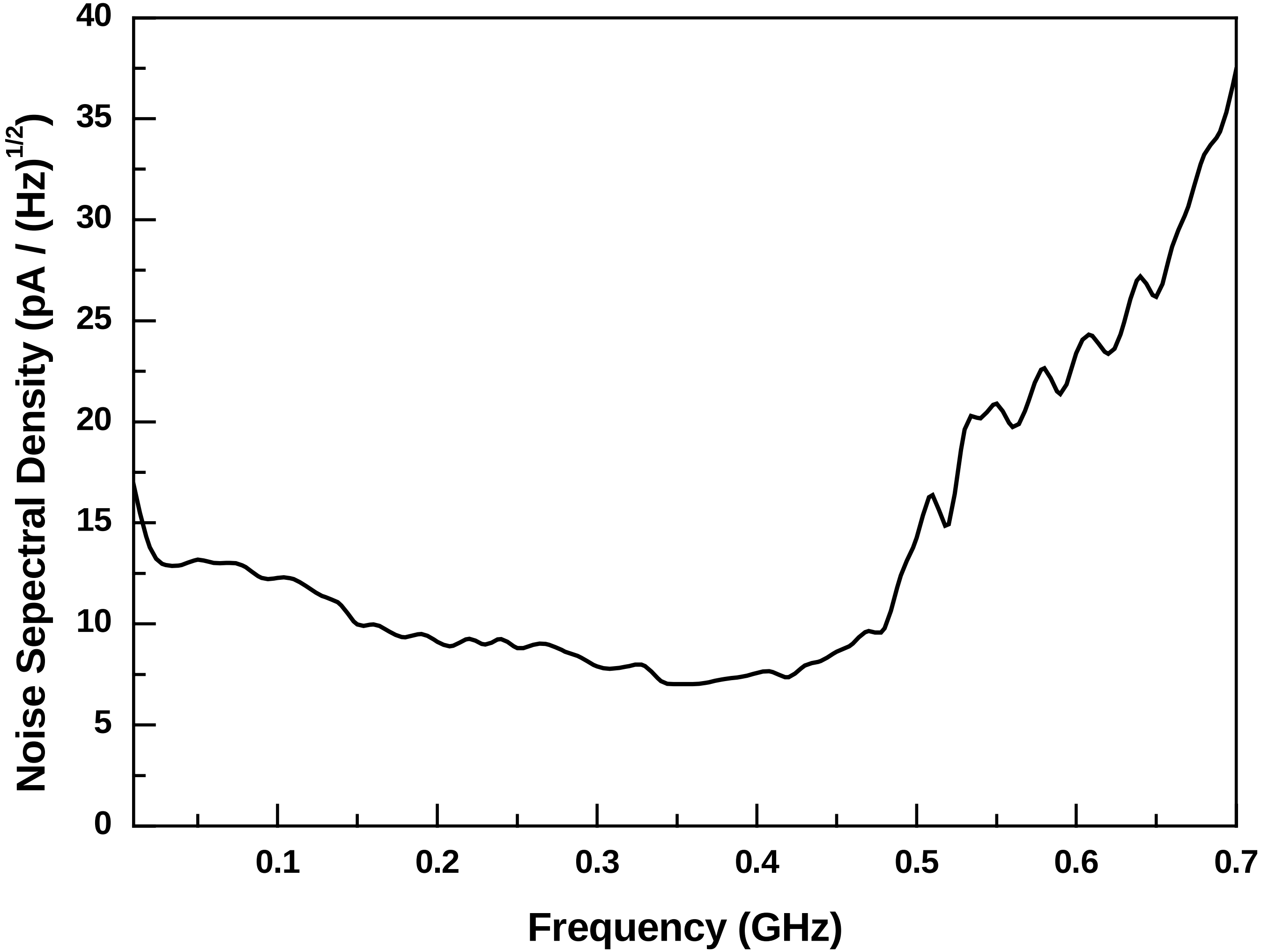
Gain & Bandwidth



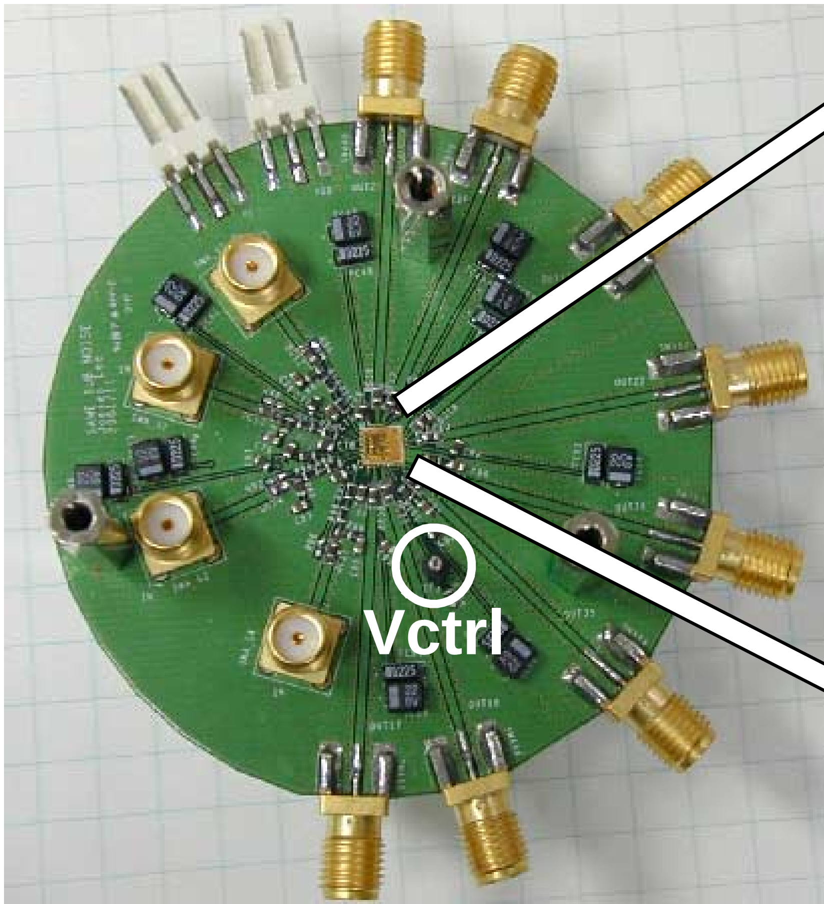
Crosstalk

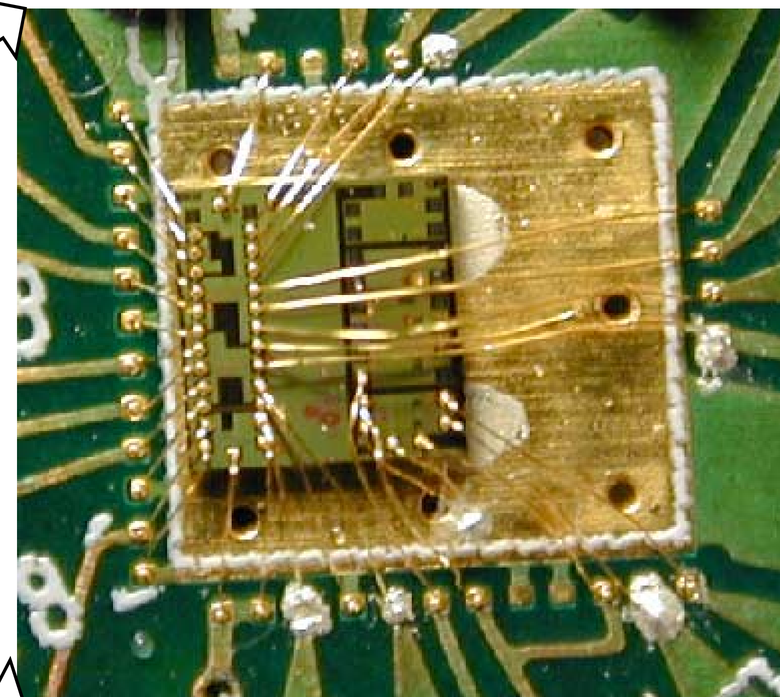

90
80
70
60
50
40
30
20
10
0
0.3
1
Relative Response (dBΩ)
Frequency (GHz)
Signal Gain
< - 40dB
Crosstalk

Noise Current



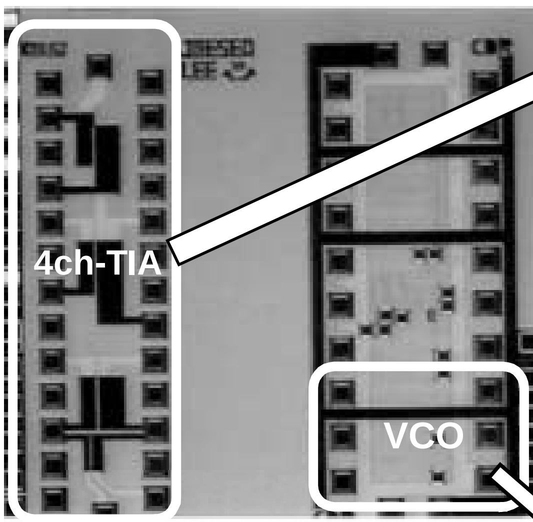
Digital noise ***test board***

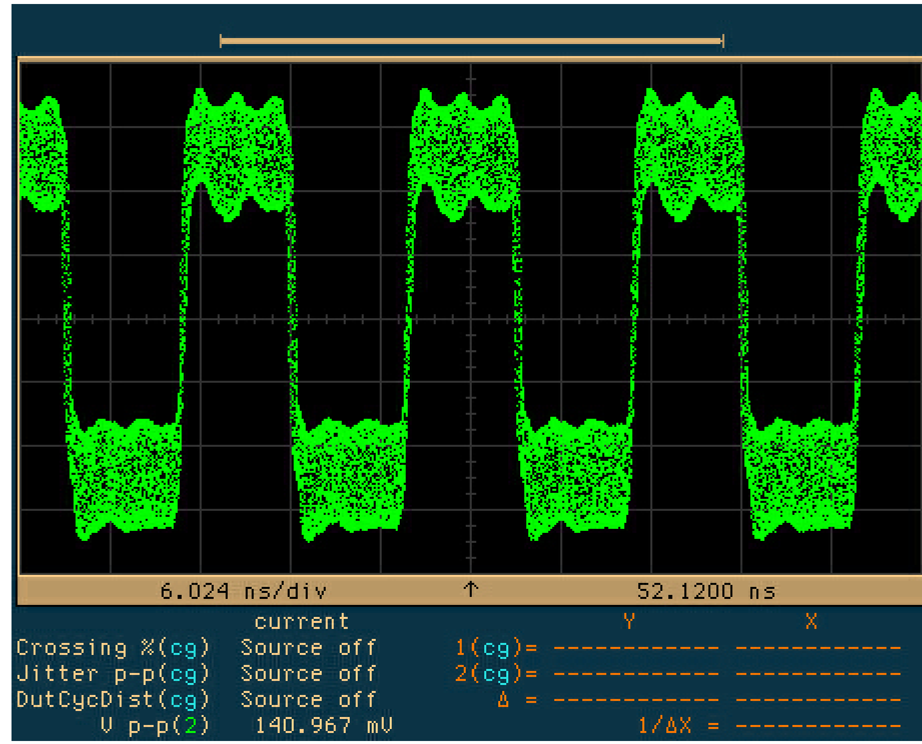




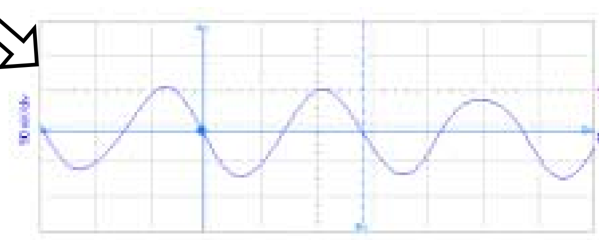
- **4-Layer PCB**

Digital noise through same substrate



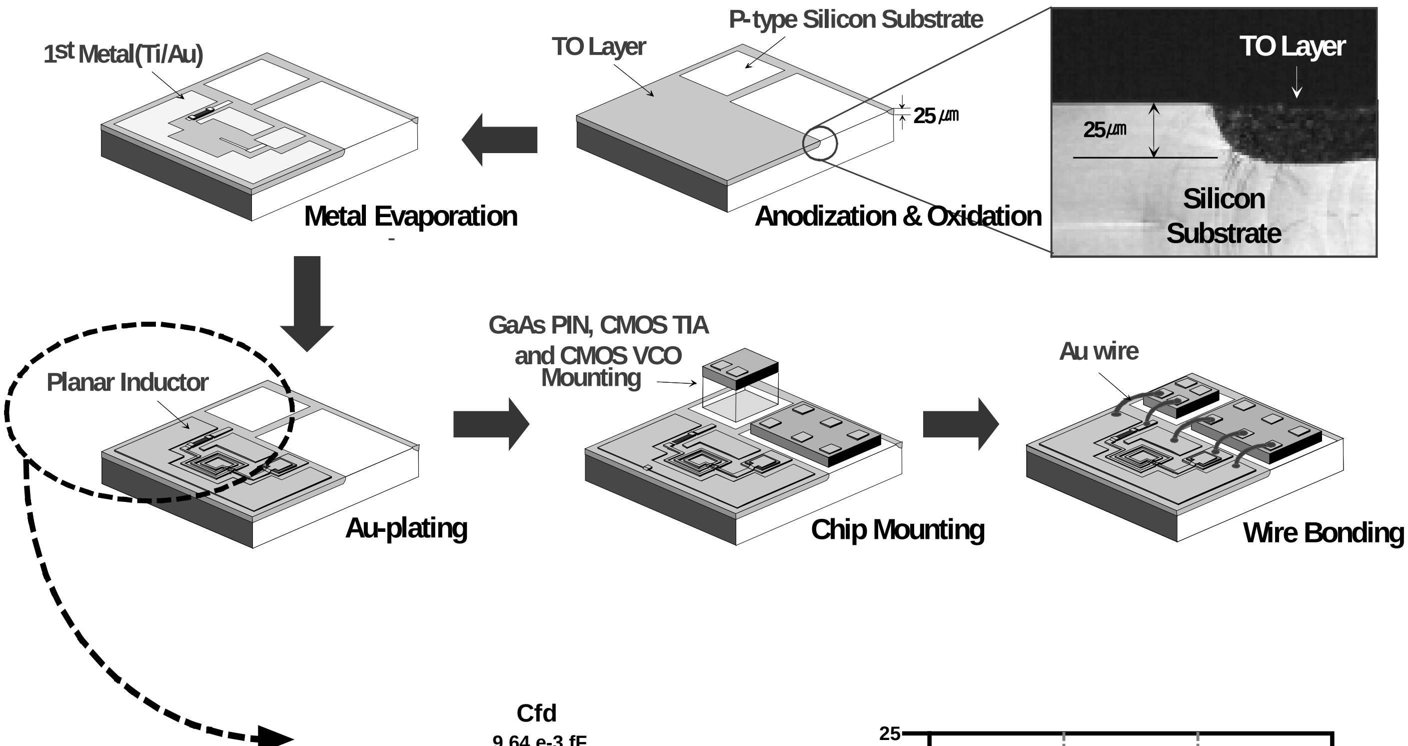


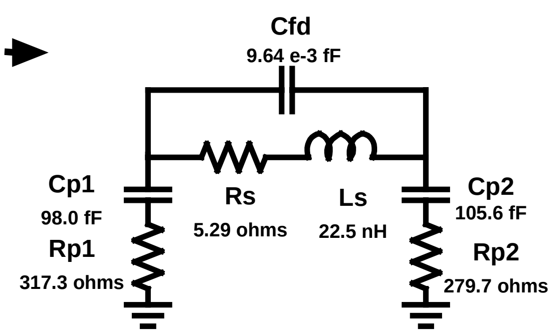
Process:
Retrograde twin well



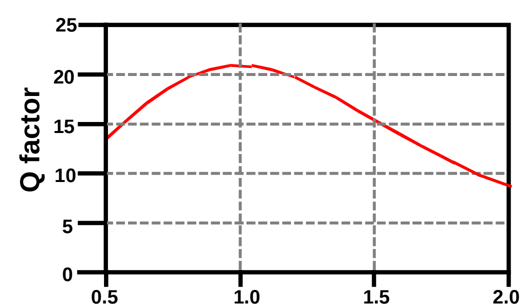
Output at Vctrl=1.2V

Multichip on Oxide (MCO) Process

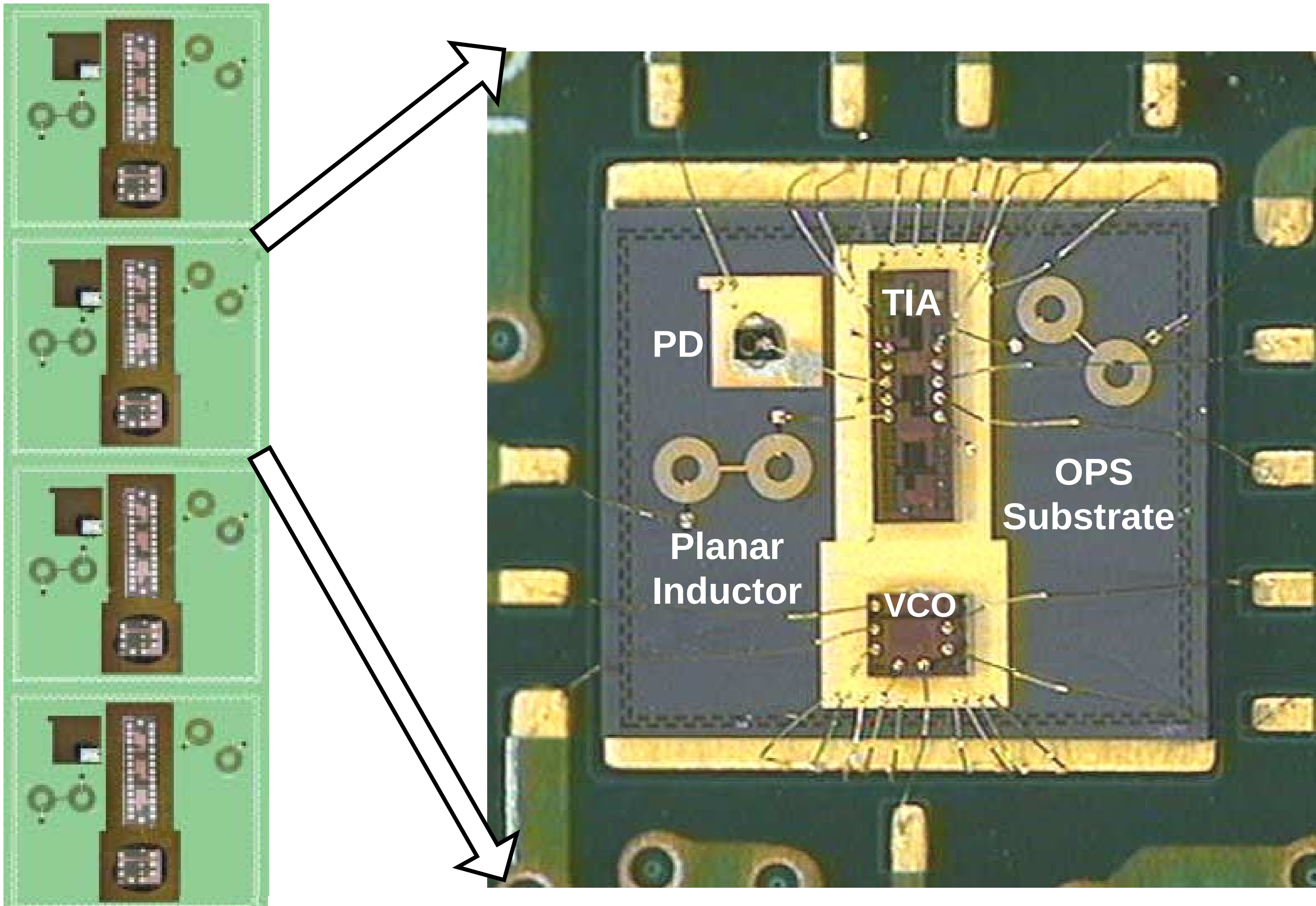




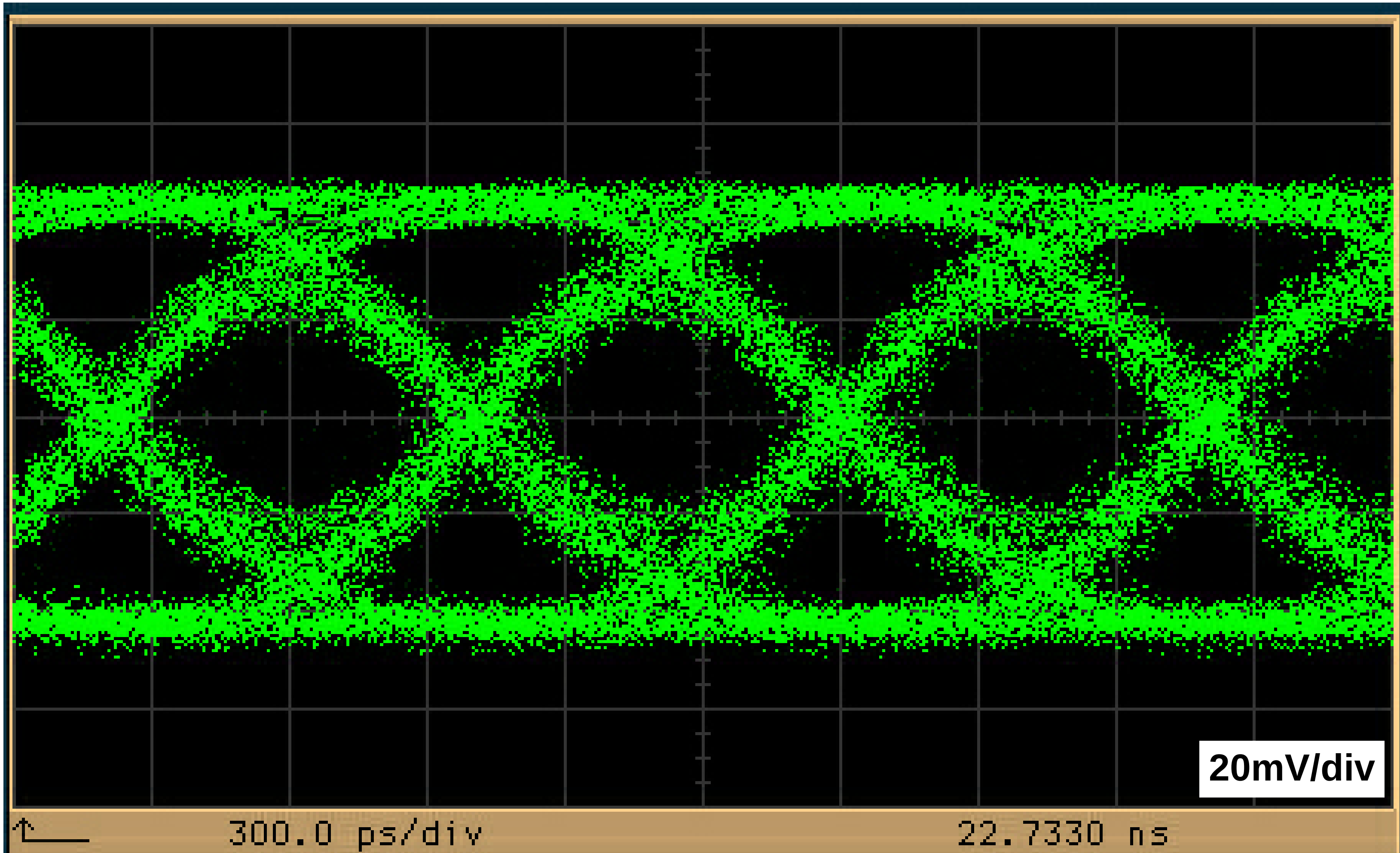
Equivalent circuits



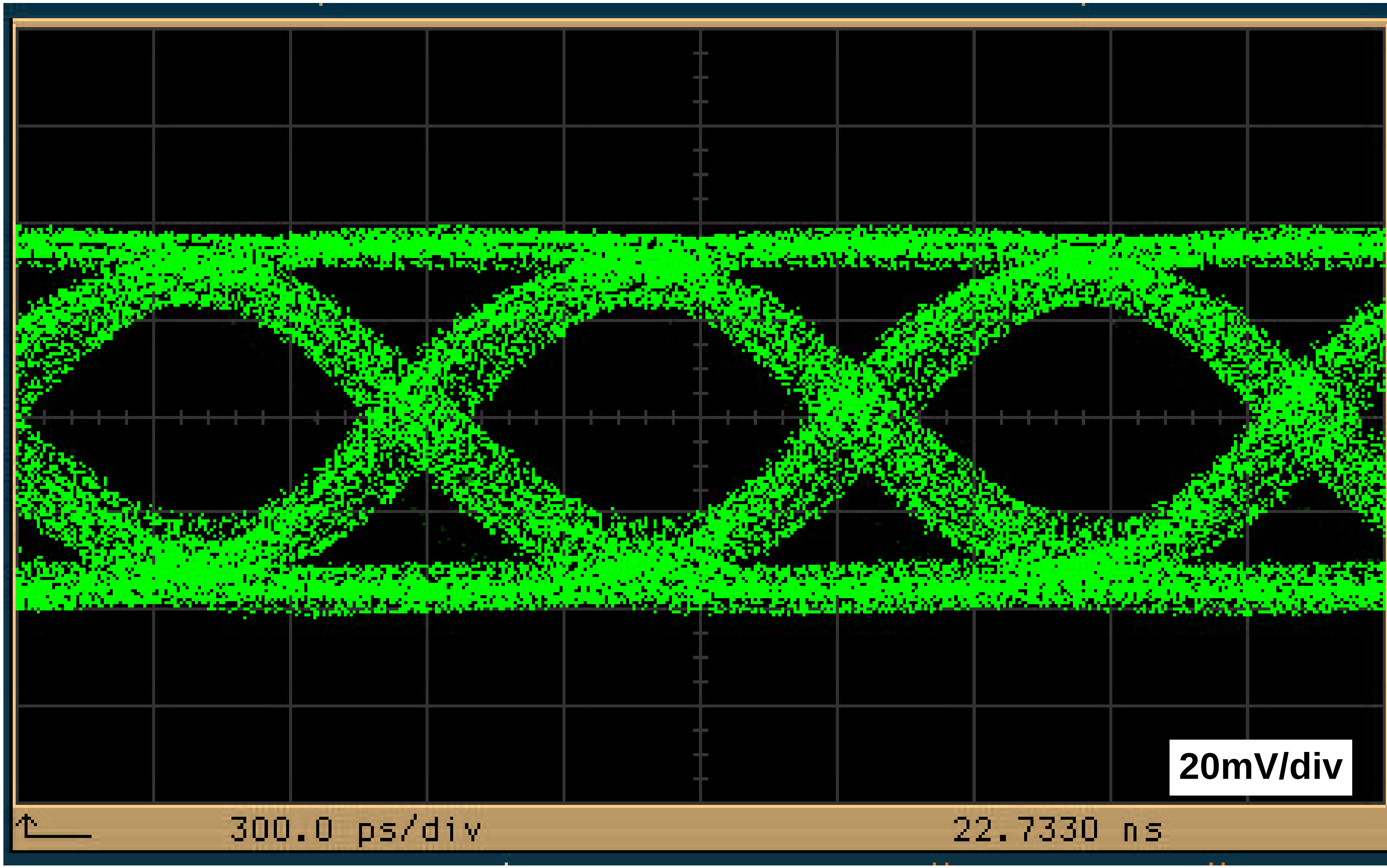
MCO Chip microphotograph



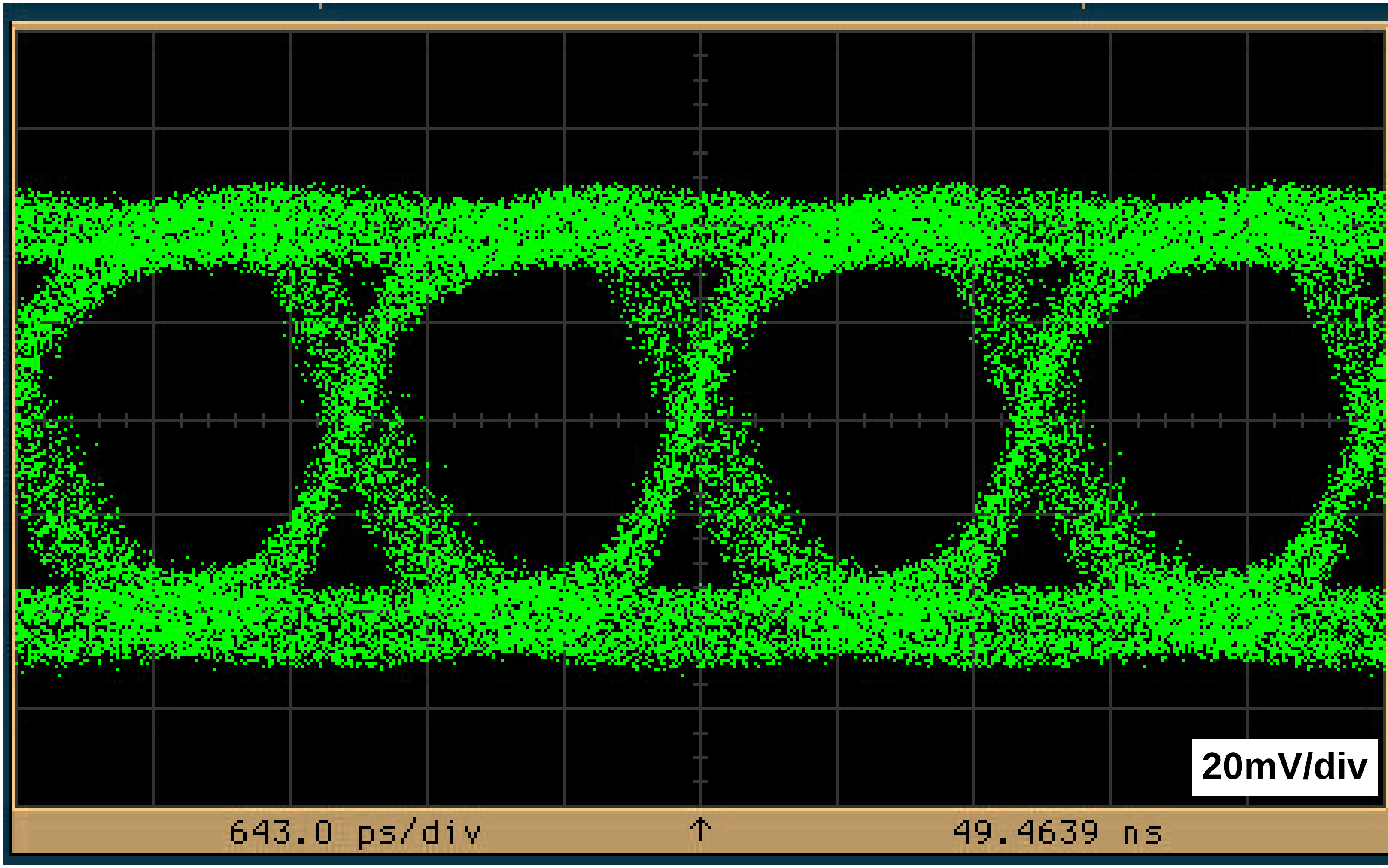
Eye-diagram – 1.25Gbps



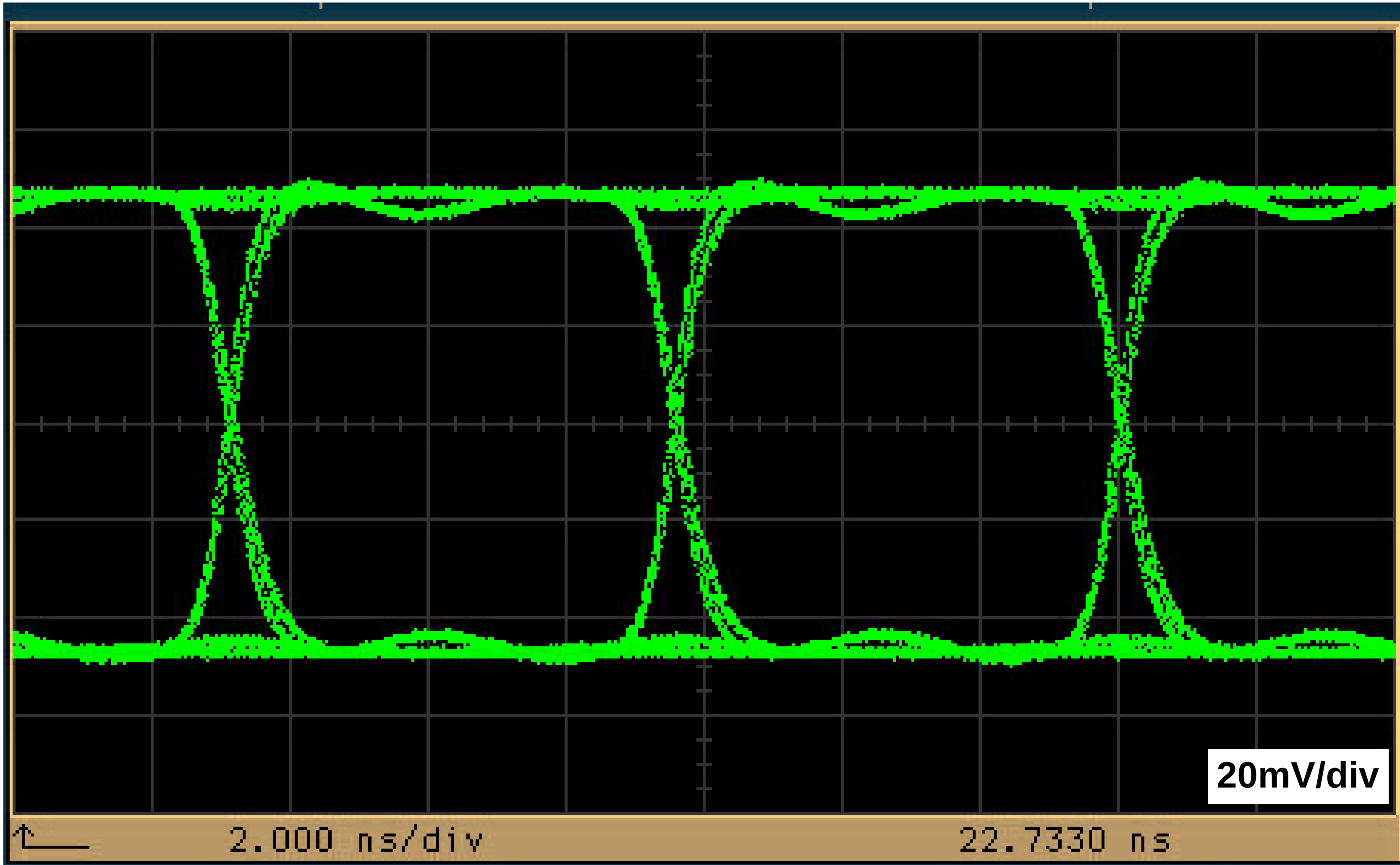
Eye-diagram – 1.022Gbps



Eye-diagram – 622Mbps



Eye-diagram – 155Mbps



Performance summary

Supply voltage	2.5V
Power consumption	27mW
Bandwidth(3dB)	670MHz
Photodiode capacitance	1pF
Noise current	0.13μA
Transimpedance Gain	80dBΩ (differential)
	74dBΩ (single-ended)
Max output voltage swing (single-ended)	200 mVp-p
Die area	0.13 x 0.16 mm^2 (active area of TIA) 5 x 5 mm^2 (MCM chip)
Technology	0.25μm standard CMOS

Conclusion

- Approach to One-chip Solution for Optical Receiver with Digital Noise Free
- Design and implementation of gigabit 0.25mm CMOS transimpedance amplifier for optical receiver application
- Verification through measurements